### Device Usage Page (usage\_statistics\_webtalk.html)

This HTML page displays the device usage statistics that will be sent to Xilinx.

To see the actual file transmitted to Xilinx, please click [here](http://docs.google.com/usage_statistics_webtalk.xml).

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| **software\_version\_and\_target\_device** | | | |
| **beta** | FALSE | **build\_version** | 1909853 |
| **date\_generated** | Wed Jan 23 16:13:24 2019 | **os\_platform** | WIN64 |
| **product\_version** | Vivado v2017.2 (64-bit) | **project\_id** | 27dadd15a4ce4d8d87a07bc80d23f169 |
| **project\_iteration** | 1 | **random\_id** | d4a2cac2d54657e7bee09ddc0da13754 |
| **registration\_id** | d4a2cac2d54657e7bee09ddc0da13754 | **route\_design** | TRUE |
| **target\_device** | xc7a100t | **target\_family** | artix7 |
| **target\_package** | csg324 | **target\_speed** | -1 |
| **tool\_flow** | Vivado |

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| **user\_environment** | | | |
| **cpu\_name** | Intel(R) Core(TM) i7-6700K CPU @ 4.00GHz | **cpu\_speed** | 4008 MHz |
| **os\_name** | Microsoft Windows 8 or later , 64-bit | **os\_release** | major release (build 9200) |
| **system\_ram** | 17.000 GB | **total\_processors** | 1 |

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| **vivado\_usage** | | | |

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| **java\_command\_handlers** | | | |
| addsources=5 | newproject=1 | runbitgen=4 | runimplementation=1 |
| runsynthesis=1 | showview=1 | toolssettings=1 |

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| **other\_data** | | | |
| guimode=1 |

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| **project\_data** | | | |
| constraintsetcount=1 | core\_container=false | currentimplrun=impl\_1 | currentsynthesisrun=synth\_1 |
| default\_library=xil\_defaultlib | designmode=RTL | export\_simulation\_activehdl=0 | export\_simulation\_ies=0 |
| export\_simulation\_modelsim=0 | export\_simulation\_questa=0 | export\_simulation\_riviera=0 | export\_simulation\_vcs=0 |
| export\_simulation\_xsim=0 | implstrategy=Vivado Implementation Defaults | launch\_simulation\_activehdl=0 | launch\_simulation\_ies=0 |
| launch\_simulation\_modelsim=0 | launch\_simulation\_questa=0 | launch\_simulation\_riviera=0 | launch\_simulation\_vcs=0 |
| launch\_simulation\_xsim=0 | simulator\_language=Verilog | srcsetcount=1 | synthesisstrategy=Vivado Synthesis Defaults |
| target\_language=Verilog | target\_simulator=XSim | totalimplruns=1 | totalsynthesisruns=1 |

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| **unisim\_transformation** |
| |  |  |  |  | | --- | --- | --- | --- | | **post\_unisim\_transformation** | | | | | ibuf=2 | lut2=1 | obuf=1 | |
| |  |  |  |  | | --- | --- | --- | --- | | **pre\_unisim\_transformation** | | | | | ibuf=2 | lut2=1 | obuf=1 | |

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| **report\_drc** |
| |  |  |  |  | | --- | --- | --- | --- | | **command\_line\_options** | | | | | -append=default::[not\_specified] | -checks=default::[not\_specified] | -fail\_on=default::[not\_specified] | -force=default::[not\_specified] | | -format=default::[not\_specified] | -messages=default::[not\_specified] | -name=default::[not\_specified] | -return\_string=default::[not\_specified] | | -ruledecks=default::[not\_specified] | -upgrade\_cw=default::[not\_specified] | -waived=default::[not\_specified] | |
| |  |  |  |  | | --- | --- | --- | --- | | **results** | | | | | cfgbvs-1=1 | |

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| **report\_methodology** |
| |  |  |  |  | | --- | --- | --- | --- | | **command\_line\_options** | | | | | -append=default::[not\_specified] | -checks=default::[not\_specified] | -fail\_on=default::[not\_specified] | -force=default::[not\_specified] | | -format=default::[not\_specified] | -messages=default::[not\_specified] | -name=default::[not\_specified] | -return\_string=default::[not\_specified] | | -waived=default::[not\_specified] | |

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| **report\_power** |
| |  |  |  |  | | --- | --- | --- | --- | | **command\_line\_options** | | | | | -advisory=default::[not\_specified] | -append=default::[not\_specified] | -file=[specified] | -format=default::text | | -hier=default::power | -l=default::[not\_specified] | -name=default::[not\_specified] | -no\_propagation=default::[not\_specified] | | -return\_string=default::[not\_specified] | -rpx=[specified] | -verbose=default::[not\_specified] | -vid=default::[not\_specified] | | -xpe=default::[not\_specified] | |
| |  |  |  |  | | --- | --- | --- | --- | | **usage** | | | | | airflow=250 (LFM) | ambient\_temp=25.0 (C) | bi-dir\_toggle=12.500000 | bidir\_output\_enable=1.000000 | | board\_layers=12to15 (12 to 15 Layers) | board\_selection=medium (10"x10") | confidence\_level\_clock\_activity=High | confidence\_level\_design\_state=High | | confidence\_level\_device\_models=High | confidence\_level\_internal\_activity=Medium | confidence\_level\_io\_activity=Low | confidence\_level\_overall=Low | | customer=TBD | customer\_class=TBD | devstatic=0.099409 | die=xc7a100tcsg324-1 | | dsp\_output\_toggle=12.500000 | dynamic=0.701686 | effective\_thetaja=4.6 | enable\_probability=0.990000 | | family=artix7 | ff\_toggle=12.500000 | flow\_state=routed | heatsink=medium (Medium Profile) | | i/o=0.691146 | input\_toggle=12.500000 | junction\_temp=28.7 (C) | logic=0.001370 | | mgtavcc\_dynamic\_current=0.000000 | mgtavcc\_static\_current=0.000000 | mgtavcc\_total\_current=0.000000 | mgtavcc\_voltage=1.000000 | | mgtavtt\_dynamic\_current=0.000000 | mgtavtt\_static\_current=0.000000 | mgtavtt\_total\_current=0.000000 | mgtavtt\_voltage=1.200000 | | netlist\_net\_matched=NA | off-chip\_power=0.000000 | on-chip\_power=0.801095 | output\_enable=1.000000 | | output\_load=5.000000 | output\_toggle=12.500000 | package=csg324 | pct\_clock\_constrained=1.000000 | | pct\_inputs\_defined=0 | platform=nt64 | process=typical | ram\_enable=50.000000 | | ram\_write=50.000000 | read\_saif=False | set/reset\_probability=0.000000 | signal\_rate=False | | signals=0.009170 | simulation\_file=None | speedgrade=-1 | static\_prob=False | | temp\_grade=commercial | thetajb=5.7 (C/W) | thetasa=4.6 (C/W) | toggle\_rate=False | | user\_board\_temp=25.0 (C) | user\_effective\_thetaja=4.6 | user\_junc\_temp=28.7 (C) | user\_thetajb=5.7 (C/W) | | user\_thetasa=4.6 (C/W) | vccadc\_dynamic\_current=0.000000 | vccadc\_static\_current=0.020000 | vccadc\_total\_current=0.020000 | | vccadc\_voltage=1.800000 | vccaux\_dynamic\_current=0.025033 | vccaux\_io\_dynamic\_current=0.000000 | vccaux\_io\_static\_current=0.000000 | | vccaux\_io\_total\_current=0.000000 | vccaux\_io\_voltage=1.800000 | vccaux\_static\_current=0.018310 | vccaux\_total\_current=0.043343 | | vccaux\_voltage=1.800000 | vccbram\_dynamic\_current=0.000000 | vccbram\_static\_current=0.000280 | vccbram\_total\_current=0.000280 | | vccbram\_voltage=1.000000 | vccint\_dynamic\_current=0.018540 | vccint\_static\_current=0.016972 | vccint\_total\_current=0.035512 | | vccint\_voltage=1.000000 | vcco12\_dynamic\_current=0.000000 | vcco12\_static\_current=0.000000 | vcco12\_total\_current=0.000000 | | vcco12\_voltage=1.200000 | vcco135\_dynamic\_current=0.000000 | vcco135\_static\_current=0.000000 | vcco135\_total\_current=0.000000 | | vcco135\_voltage=1.350000 | vcco15\_dynamic\_current=0.000000 | vcco15\_static\_current=0.000000 | vcco15\_total\_current=0.000000 | | vcco15\_voltage=1.500000 | vcco18\_dynamic\_current=0.000000 | vcco18\_static\_current=0.000000 | vcco18\_total\_current=0.000000 | | vcco18\_voltage=1.800000 | vcco25\_dynamic\_current=0.000000 | vcco25\_static\_current=0.000000 | vcco25\_total\_current=0.000000 | | vcco25\_voltage=2.500000 | vcco33\_dynamic\_current=0.193359 | vcco33\_static\_current=0.004000 | vcco33\_total\_current=0.197359 | | vcco33\_voltage=3.300000 | version=2017.2 | |

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| **report\_utilization** |
| |  |  |  |  | | --- | --- | --- | --- | | **clocking** | | | | | bufgctrl\_available=32 | bufgctrl\_fixed=0 | bufgctrl\_used=0 | bufgctrl\_util\_percentage=0.00 | | bufhce\_available=96 | bufhce\_fixed=0 | bufhce\_used=0 | bufhce\_util\_percentage=0.00 | | bufio\_available=24 | bufio\_fixed=0 | bufio\_used=0 | bufio\_util\_percentage=0.00 | | bufmrce\_available=12 | bufmrce\_fixed=0 | bufmrce\_used=0 | bufmrce\_util\_percentage=0.00 | | bufr\_available=24 | bufr\_fixed=0 | bufr\_used=0 | bufr\_util\_percentage=0.00 | | mmcme2\_adv\_available=6 | mmcme2\_adv\_fixed=0 | mmcme2\_adv\_used=0 | mmcme2\_adv\_util\_percentage=0.00 | | plle2\_adv\_available=6 | plle2\_adv\_fixed=0 | plle2\_adv\_used=0 | plle2\_adv\_util\_percentage=0.00 | |
| |  |  |  |  | | --- | --- | --- | --- | | **dsp** | | | | | dsps\_available=240 | dsps\_fixed=0 | dsps\_used=0 | dsps\_util\_percentage=0.00 | |
| |  |  |  |  | | --- | --- | --- | --- | | **io\_standard** | | | | | blvds\_25=0 | diff\_hstl\_i=0 | diff\_hstl\_i\_18=0 | diff\_hstl\_ii=0 | | diff\_hstl\_ii\_18=0 | diff\_hsul\_12=0 | diff\_mobile\_ddr=0 | diff\_sstl135=0 | | diff\_sstl135\_r=0 | diff\_sstl15=0 | diff\_sstl15\_r=0 | diff\_sstl18\_i=0 | | diff\_sstl18\_ii=0 | hstl\_i=0 | hstl\_i\_18=0 | hstl\_ii=0 | | hstl\_ii\_18=0 | hsul\_12=0 | lvcmos12=0 | lvcmos15=0 | | lvcmos18=0 | lvcmos25=0 | lvcmos33=1 | lvds\_25=0 | | lvttl=0 | mini\_lvds\_25=0 | mobile\_ddr=0 | pci33\_3=0 | | ppds\_25=0 | rsds\_25=0 | sstl135=0 | sstl135\_r=0 | | sstl15=0 | sstl15\_r=0 | sstl18\_i=0 | sstl18\_ii=0 | | tmds\_33=0 | |
| |  |  |  |  | | --- | --- | --- | --- | | **memory** | | | | | block\_ram\_tile\_available=135 | block\_ram\_tile\_fixed=0 | block\_ram\_tile\_used=0 | block\_ram\_tile\_util\_percentage=0.00 | | ramb18\_available=270 | ramb18\_fixed=0 | ramb18\_used=0 | ramb18\_util\_percentage=0.00 | | ramb36\_fifo\_available=135 | ramb36\_fifo\_fixed=0 | ramb36\_fifo\_used=0 | ramb36\_fifo\_util\_percentage=0.00 | |
| |  |  |  |  | | --- | --- | --- | --- | | **primitives** | | | | | ibuf\_functional\_category=IO | ibuf\_used=2 | lut2\_functional\_category=LUT | lut2\_used=1 | | obuf\_functional\_category=IO | obuf\_used=1 | |
| |  |  |  |  | | --- | --- | --- | --- | | **slice\_logic** | | | | | f7\_muxes\_available=31700 | f7\_muxes\_fixed=0 | f7\_muxes\_used=0 | f7\_muxes\_util\_percentage=0.00 | | f8\_muxes\_available=15850 | f8\_muxes\_fixed=0 | f8\_muxes\_used=0 | f8\_muxes\_util\_percentage=0.00 | | lut\_as\_logic\_available=63400 | lut\_as\_logic\_fixed=0 | lut\_as\_logic\_used=1 | lut\_as\_logic\_util\_percentage=<0.01 | | lut\_as\_memory\_available=19000 | lut\_as\_memory\_fixed=0 | lut\_as\_memory\_used=0 | lut\_as\_memory\_util\_percentage=0.00 | | register\_as\_flip\_flop\_available=126800 | register\_as\_flip\_flop\_fixed=0 | register\_as\_flip\_flop\_used=0 | register\_as\_flip\_flop\_util\_percentage=0.00 | | register\_as\_latch\_available=126800 | register\_as\_latch\_fixed=0 | register\_as\_latch\_used=0 | register\_as\_latch\_util\_percentage=0.00 | | slice\_luts\_available=63400 | slice\_luts\_fixed=0 | slice\_luts\_used=1 | slice\_luts\_util\_percentage=<0.01 | | slice\_registers\_available=126800 | slice\_registers\_fixed=0 | slice\_registers\_used=0 | slice\_registers\_util\_percentage=0.00 | | lut\_as\_distributed\_ram\_fixed=0 | lut\_as\_distributed\_ram\_used=0 | lut\_as\_logic\_available=63400 | lut\_as\_logic\_fixed=0 | | lut\_as\_logic\_used=1 | lut\_as\_logic\_util\_percentage=<0.01 | lut\_as\_memory\_available=19000 | lut\_as\_memory\_fixed=0 | | lut\_as\_memory\_used=0 | lut\_as\_memory\_util\_percentage=0.00 | lut\_as\_shift\_register\_fixed=0 | lut\_as\_shift\_register\_used=0 | | lut\_flip\_flop\_pairs\_available=63400 | lut\_flip\_flop\_pairs\_fixed=0 | lut\_flip\_flop\_pairs\_used=0 | lut\_flip\_flop\_pairs\_util\_percentage=0.00 | | slice\_available=15850 | slice\_fixed=0 | slice\_used=1 | slice\_util\_percentage=<0.01 | | slicel\_fixed=0 | slicel\_used=1 | slicem\_fixed=0 | slicem\_used=0 | | unique\_control\_sets\_used=0 | using\_o5\_and\_o6\_fixed=0 | using\_o5\_and\_o6\_used=0 | using\_o5\_output\_only\_fixed=0 | | using\_o5\_output\_only\_used=0 | using\_o6\_output\_only\_fixed=0 | using\_o6\_output\_only\_used=1 | |
| |  |  |  |  | | --- | --- | --- | --- | | **specific\_feature** | | | | | bscane2\_available=4 | bscane2\_fixed=0 | bscane2\_used=0 | bscane2\_util\_percentage=0.00 | | capturee2\_available=1 | capturee2\_fixed=0 | capturee2\_used=0 | capturee2\_util\_percentage=0.00 | | dna\_port\_available=1 | dna\_port\_fixed=0 | dna\_port\_used=0 | dna\_port\_util\_percentage=0.00 | | efuse\_usr\_available=1 | efuse\_usr\_fixed=0 | efuse\_usr\_used=0 | efuse\_usr\_util\_percentage=0.00 | | frame\_ecce2\_available=1 | frame\_ecce2\_fixed=0 | frame\_ecce2\_used=0 | frame\_ecce2\_util\_percentage=0.00 | | icape2\_available=2 | icape2\_fixed=0 | icape2\_used=0 | icape2\_util\_percentage=0.00 | | pcie\_2\_1\_available=1 | pcie\_2\_1\_fixed=0 | pcie\_2\_1\_used=0 | pcie\_2\_1\_util\_percentage=0.00 | | startupe2\_available=1 | startupe2\_fixed=0 | startupe2\_used=0 | startupe2\_util\_percentage=0.00 | | xadc\_available=1 | xadc\_fixed=0 | xadc\_used=0 | xadc\_util\_percentage=0.00 | |

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| **router** |
| |  |  |  |  | | --- | --- | --- | --- | | **usage** | | | | | actual\_expansions=281 | bogomips=0 | bram18=0 | bram36=0 | | bufg=0 | bufr=0 | ctrls=0 | dsp=0 | | effort=2 | estimated\_expansions=3366 | ff=0 | global\_clocks=0 | | high\_fanout\_nets=0 | iob=3 | lut=1 | movable\_instances=4 | | nets=6 | pins=9 | pll=0 | router\_runtime=0.000000 | | router\_timing\_driven=1 | threads=2 | timing\_constraints\_exist=1 | |

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| **synthesis** |
| |  |  |  |  | | --- | --- | --- | --- | | **command\_line\_options** | | | | | -assert=default::[not\_specified] | -bufg=default::12 | -cascade\_dsp=default::auto | -constrset=default::[not\_specified] | | -control\_set\_opt\_threshold=default::auto | -directive=default::default | -fanout\_limit=default::10000 | -flatten\_hierarchy=default::rebuilt | | -fsm\_extraction=default::auto | -gated\_clock\_conversion=default::off | -generic=default::[not\_specified] | -include\_dirs=default::[not\_specified] | | -keep\_equivalent\_registers=default::[not\_specified] | -max\_bram=default::-1 | -max\_bram\_cascade\_height=default::-1 | -max\_dsp=default::-1 | | -max\_uram=default::-1 | -max\_uram\_cascade\_height=default::-1 | -mode=default::default | -name=default::[not\_specified] | | -no\_lc=default::[not\_specified] | -no\_srlextract=default::[not\_specified] | -no\_timing\_driven=default::[not\_specified] | -part=xc7a100tcsg324-1 | | -resource\_sharing=default::auto | -retiming=default::[not\_specified] | -rtl=default::[not\_specified] | -rtl\_skip\_constraints=default::[not\_specified] | | -rtl\_skip\_ip=default::[not\_specified] | -seu\_protect=default::none | -sfcu=default::[not\_specified] | -shreg\_min\_size=default::3 | | -top=myand | -verilog\_define=default::[not\_specified] | |
| |  |  |  |  | | --- | --- | --- | --- | | **usage** | | | | | elapsed=00:00:20s | hls\_ip=0 | memory\_gain=404.387MB | memory\_peak=627.586MB | |